

FIGI

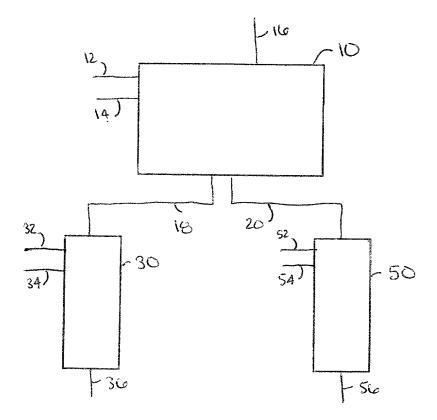
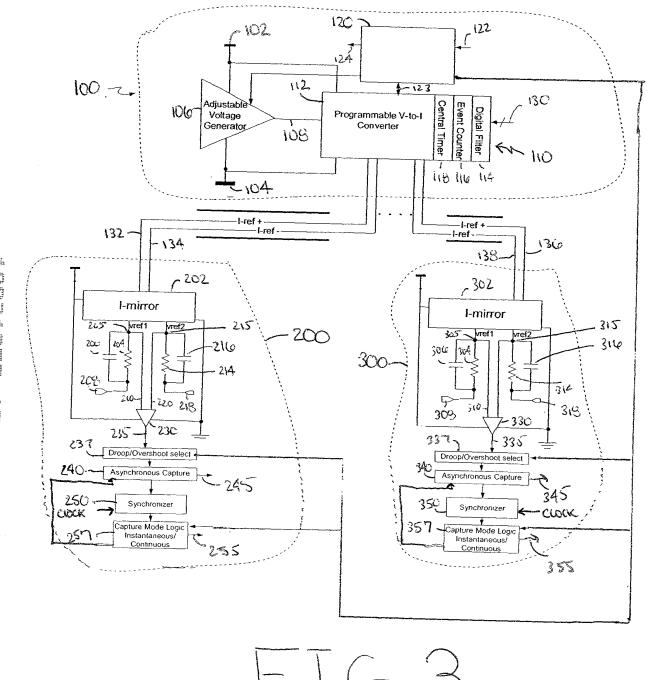


FIG. 2



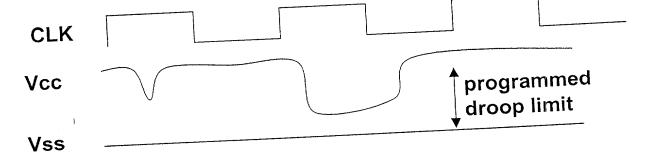
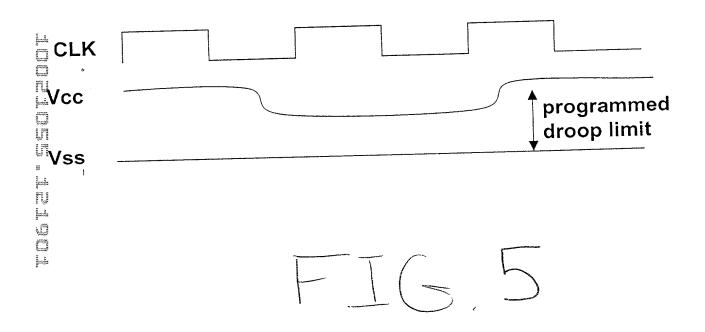


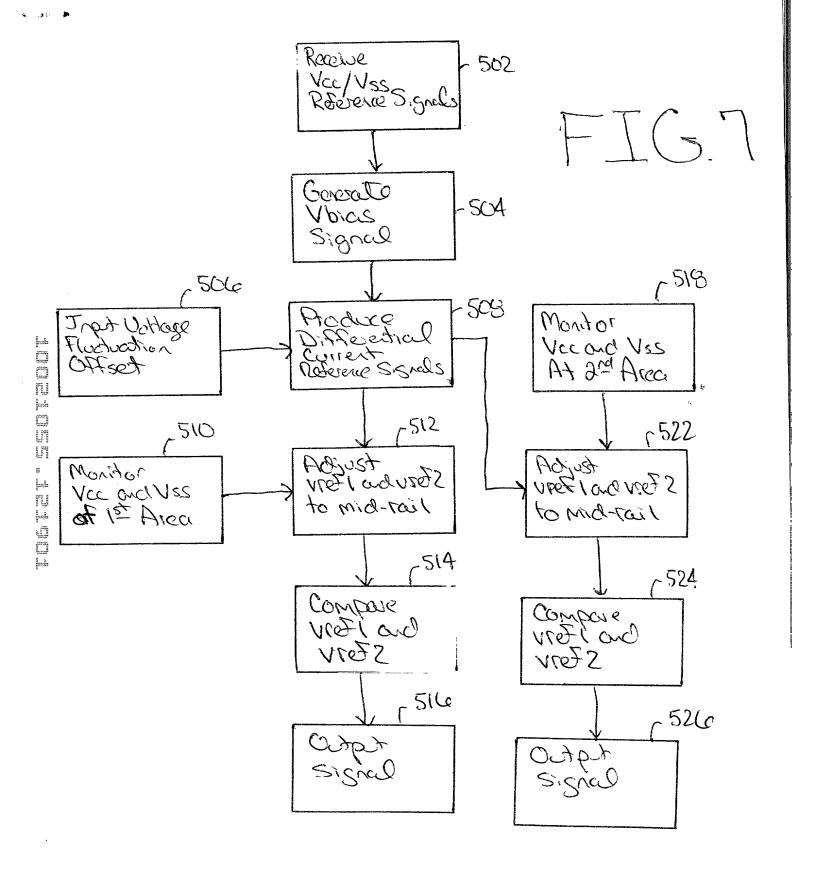
FIG. A



CLK (core clock does not need to be ON)

Vcc programmed droop limit

Vss



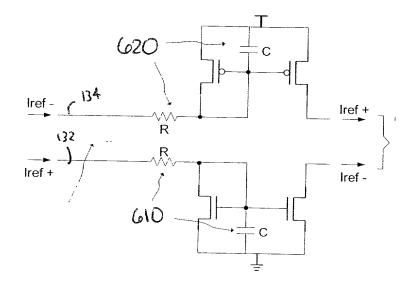


FIG8